IDEC Chip Design Contest

Design of Reconfigurable 12~14-bit Hybrid SAR-SS Analog to Digital Converter with SS Bit Shifting Method

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Introduction

This paper proposes a SAR-SS hybrid ADC structure that can reconfigure resolution for a bio-signal processing system used in wearable devices. The SAR ADC is placed in the MSB 8-10 bits, and the SS ADC is placed in the LSB 4 bits to implement a total resolution of 12, 13, 14 bits, and resolution can be reconfigured by an external signal(C1, C0) using a Bit Shifting method.

Top Cell & Layout

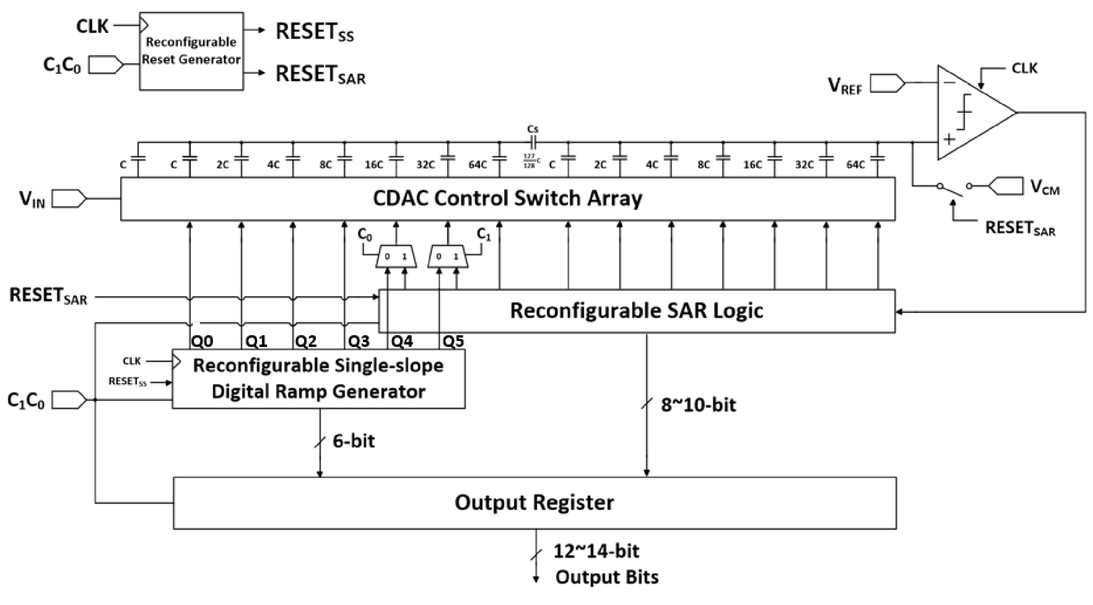

Fig. 1. Block diagram of the proposed 11-14 SAR/SS ADC

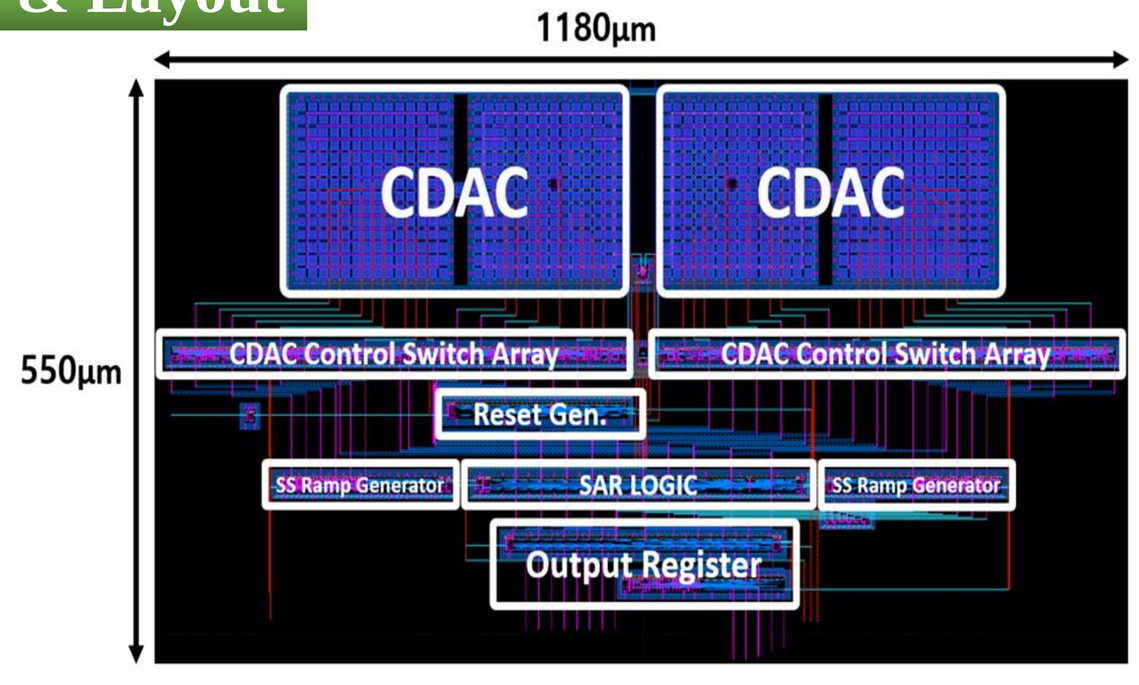

Fig. 2. Proposed ADC Layout

Measurement result & Description

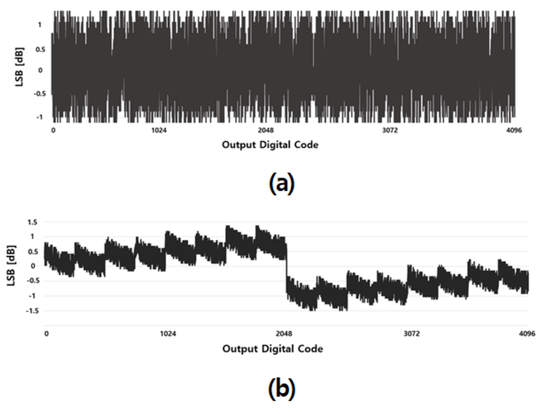

Fig. 3. (a)DNL (b)INL

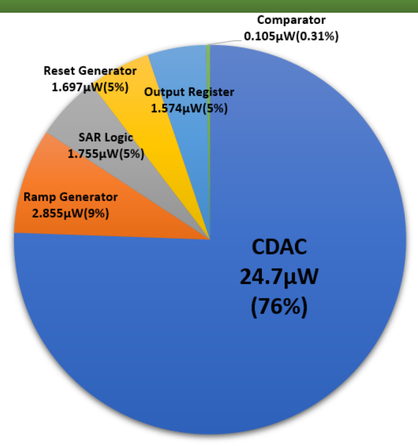

Fig 4. Power Consumption

SAR logic is connected only to the top 10 bits of the capacitor DAC, and a single slope digital lamp signal generator is connected to the bottom 6-bits to apply a 4-bit binary signal.

The output stage of the single-slope digital ramp generator produces a total of six outputs(Q5~Q0). The resolution of the N-bit SAR Logic (N = 8~10) is determined by the C1 and C0 signals.

Table 1. Chip Measurement Result

Parameter	This work		
Process	28nm		
Architecture	SAR-SS		
Supply Voltage [V]	1		
Resolution [bit]	12	13	14
SNDR [dB]	66.2	70.01	72.5
ENoB [bit]	10.7	11.3	11.7
Sampling rate [S/s]	384k	370k	357k
DNL [bit]	-1.1/1.4	-1.3/1.5	-1.7/1.8
INL [bit]	1.4/-1.5	1.6/-1.5	1.9/-1.8
Power [uW]	26.8	31.1	32.7
FoM* [fJ/step]	41.9	33.3	27.5

*FoM = [Power] / ([Sampling rate] × 2^[Resolution])

Table 2. Resolution of SAR Logic and Total ADC

C0,C1	SAR bit	Total bit	Q5	Q4	Q3	Q2	Q1	Q0
00	8	12	SS3	SS2	SS1	SS0	VSS	VSS
10	9	13	VSS	SS3	SS2	SS1	SS0	VSS
11	10	14	VSS	VSS	SS3	SS2	SS1	SS0

*C1, C0 is resolution control signal.

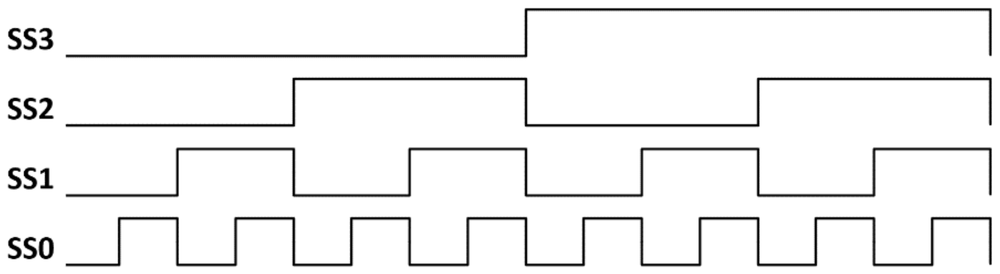

Fig 5. Binary counter output

Conclusion

Circuit is designed reconfigurable in 12,13,14 bits. The SAR ADC is designed to be reconfigurable from 8 to 10 bits, and the SS ADC is fixed at 4 bits. This ADC is used the bit shifting method. The proposed ADC uses a CMOS 28nm 1-poly 8-metal process, and the layout area is 1180um × 550um, Supply voltage is 1V.

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